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DIGITAL DOWN CONVERTER (DDC) WITH CIC FILTERS FOR SDR APPLICATIONS

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Abstract:
In many software defined radio systems the signals are at high carrier frequency but with less bandwidth which, need to be processed in full digital architectures such as in FPGAs.processing at Nyquist rates make the design complicated and has limited by the highest frequency processing possible in ASIC or FPGA.The digital down converters solve this problem by using the DSP techniques.

The straight forward implementation of digital down converter requires huge arithmetic resources and limits the maximum frequency of operation. Special DSP techniques were discovered to achieve optimum performance with limited resources on FPGA.In this project a full fledged digital down conversion system will be developed in VHDL for FPGA based software defined radio applications. The project work includes study and evolution of suitable architecture and implementation. The major blocks in design would include digital I and Q carrier generators, digital mixers, decimating /interpolating CICfilters and clock distribution circuits. The blocks such as, adder, multipliers, registers and clock & control circuitry will be used in implementing these blocks.

The Modelsim Xilinx Edition (MXE) will be used for simulating the VHDL code modules .Xilinx ISEwill be used for synthesis and bit file generation. Xilinx Chip scope will be used for on chip verification of results. The applications and possible future extensions for implemented architecture will bedocumented.

Keywords*:* Digital Down Converter (DDC)[1], Cascaded Integrator-Comb (CIC) filter[2], Software Defined Radio(SDR)[3]

INTRODUCTION

In digital signal processing a digital down-converter (DDC) converts a digitized real signal centered at an intermediate frequency (IF) to a base banded complex signal centered at zero frequency. In addition to down conversion, DDC's typically decimate to a lower sampling rate, allowing follow-on signal processing by lower speed processors.

A DDC consists of three subcomponents: a direct digital synthesizer (DDS), a low-pass filter (LPF), and a down sampler (which may be integrated into the low-passfilter).

Digital Down-Converter (DDC) is a key component of digital radios. The DDC performs the frequency translation necessary to convert the high input sample rates found in a digital radio, down to lower sample rates for further and easier processing.

The DDC consists of a Numeric Controlled Oscillator (NCO) and a mixer to down convert the input signal to base band. The base band signal is then low pass filtered by a Cascaded Integrator-Comb (CIC) filter followed by two FIR decimating filters to achieve a low sample-rate.

The DDS generates a complex sinusoidal signal at the intermediate to down converting by creating a difference signal at the IF minus the DDS frequency, they also up convert, generating an unwanted signal at the sum of the two frequencies.

A fundamental part of many communications systems is Digital down Conversion (DDC). Digital radio receivers often have fast ADC converters delivering vast amounts of data; but in many cases, the signal of interest represents a small proportion of that bandwidth. A DDC allows the rest of that data to be discarded, allowing more intensive processing to be performed on the signal of interest.

As an example, consider a radio signal lying in the range 39-40MHz. The signal bandwidth is 1MHz. However, it is often digitized with a sampling rate over 100MHZ, representing in the region of 200Mbyte/second.

The DDC allows us to select the 39-40MHz band, and to shift its frequency down to base band. Once this is complete, the sampling rate can be reduced – with a 1MHz bandwidth, a sampling rate of 2.5MHz would be fine - giving a data rate of only 5Mbyte/second. This is shown in Figure1.

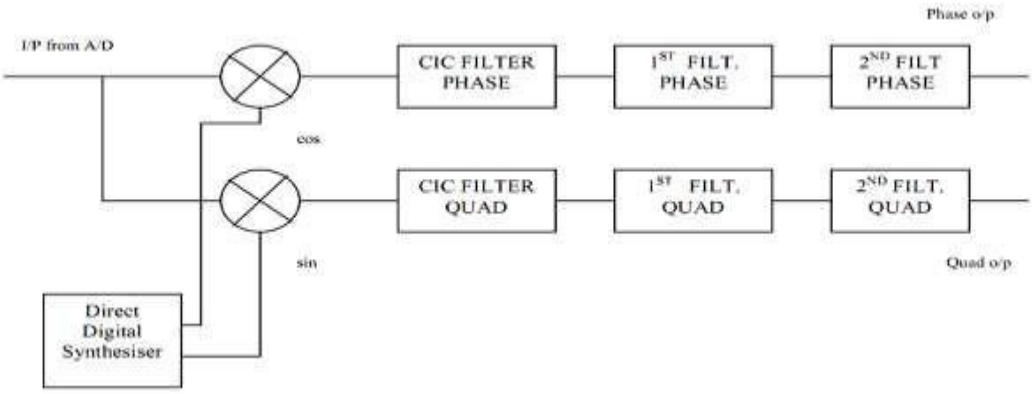


Figure1. The DDC block diagram using CIC Filters

PROPOSED DDC IMPLEMENTATION METHOD

Implementation of Decimation filter

In digital signal processing system that requires linear phase, FIR not IIR is usually used. The following is the basic structure of a decimation filter. H (n) is the anti-aliasing FIR filter.

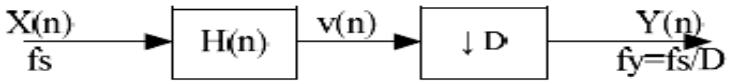


Fig2.1.1 Basic structure of a decimation filter

The FIR filter can be implemented with multiple phase structure in order to reserve resources and computation workload .the multiple phase structure is decomposed as figure 2.1.1.The decomposion of filter shows that a filter can be resolved into several branch, the order of each branch is 1/D the order of the original filter. If directly filter the h(n), each sample is computed with N order filter .But if the multiphase is applied to filter, each sample only needs to be computed with N/D order filter . So the workload of computation decreases to 1/D of the original

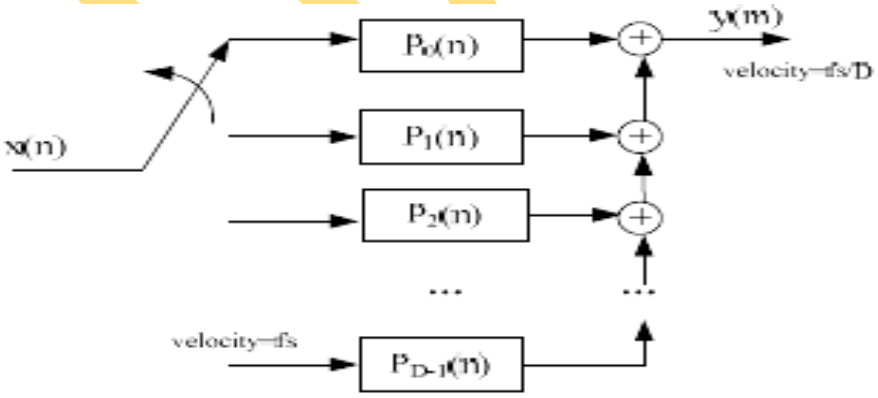


Fig2.1.2 Multiphase structure of FIR decimation filter

CIC Decimation filter

As data converters become faster and faster, the application of narrow-band extraction from wideband sources, and narrow-band construction of wideband signals is becoming more important. These functions require two basic signal processing procedures: decimation and interpolation. And while digital hardware is becoming faster, there is still the need for efficient solutions. Techniques found in very well in practice, but

large rate changes require very narrow band filters. Large rate changes require fast multipliers and very long filters. This can end up being the largest bottleneck in a DSP system.

In [Hog81], an efficient way of performing decimation and interpolation was introduced. Hogenauer devised a flexible, multiplier-free filter suitable for hardware implementation that can also handle arbitrary and large rate changes. These are known as cascaded integrator-comb filters, or CIC filters for short.

In digital signal processing, a cascaded integrator-comb (CIC) is an optimized class of finite impulse response filter combined with an interpolator or decimator.

A CIC filter consists of one or more integrator and comb filter pairs. In the case of a decimating CIC, the input signal is fed through one or more cascaded integrators, then a down-sampler, followed by one or more comb sections (equal in number to the number of integrators). An interpolating CIC is simply the reverse of this architecture, with the down-sampler replaced with a zero-stuffer (up-sampler).

CIC filters were invented by **Eugene B. Hogenauer,** and are a class of FIR filters used in multi-rate processing. The CIC filter finds applications in interpolation and decimation. Unlike most FIR filters, it has a decimator or interpolator built into the architecture. The figure at the right shows the Hogenauer architecture for a CIC Interpolator.

Cascaded integrator comb (CIC) digital filters are computationally efficient implementations of narrowband low pass filters and are often embedded in hardware implementations of decimation and interpolation in modern communications systems. CIC filters were introduced to the signal processing community, by Eugene Hogenauer, more than two decades ago, but their application possibilities have grown in recent years. Improvements in chip technology, the increased use of polyphase filtering techniques, advances in delta-sigma converter implementations, and the significant growth in wireless communications have all spurred much interest in CIC filters.

Building Blocks

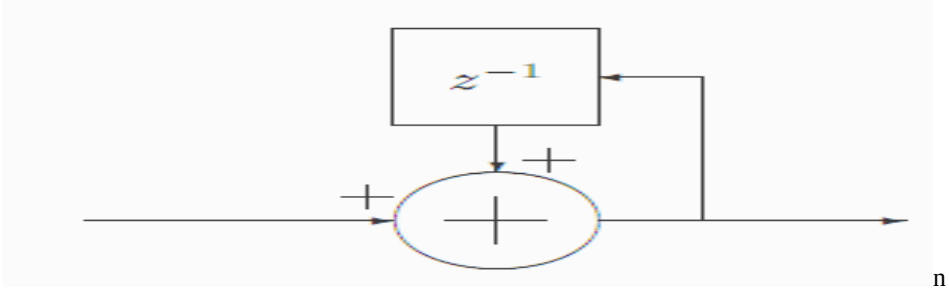
The two basic building blocks of a CIC filter are an integrator and a comb. An integrator is simply a single-pole IIR filter with a unity feedback coefficient:

$$y[n] = y[n-1] + x[n] \quad (1)$$

This system is also known as an accumulator. The transfer function for an integrator on the z- plane is

$$H_{I(Z)} = \frac{1}{1-z^{-1}} \quad (2)$$

The power response is basically a low-pass filter with a 20 dB per decade (- 6 dB per octave) roll off, but with infinite gain at DC. This is due to the single pole at z = 1; the output can grow without bound for a bounded input. In other words, a single integrator by itself is unstable.



n

Fig2.1.3.Basic Integrator

A comb filter running at the low sampling rate, f_s / R, for a rate change of R is an odd-symmetric FIR filter described by

$$y[n] = x[n] - x[n - RM] \quad (3)$$

In this equation, M is a design parameter and is called the differential delay. M can be any positive integer, but it is usually limited to 1 or 2. The corresponding transfer at f_s / R

$$H_{C(z)=1-z^{-R}} \quad (4)$$

When R = 1 and M = 1, the power response is a high-pass function with 20 dB per decade (6 dB per octave) gain(afterall,itistheinverseofanintegrator).When RM6=1,thenthepowerresponsetakesonthefamiliar raised cosine form with RM cycles from 0 to 2 π.When we build a CIC filter, we cascade, or chain output to input, N integrator sections together with N comb sections. This filter would be fine, but we can simplify it by combining it with the ratechanger.

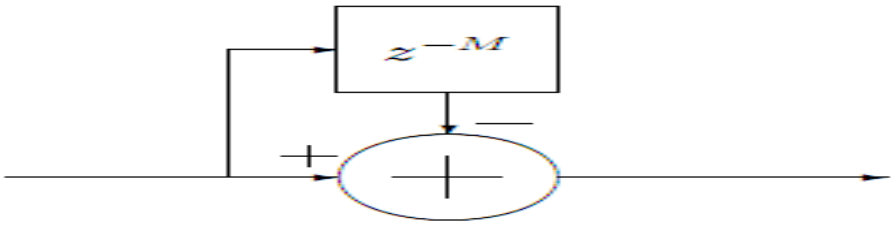


Fig2.1.4.Basic Comb

To Summarize a CIC decimator would have N cascaded integrators stages at running at clock frequency f_s, followed by a rate change by a factor R, followed by N cascaded comb stages running at f_s / R.

Fig2.1.5.Three Stage Decimating CIC Filter

Comparison with other filters

CIC filters are used in multi-rate processing. An FIR filter is used in a wide array of applications, and can be used in multi-rate processing in conjunction with an interpolator or decimator. CIC filters have low pass frequency characteristics, while FIR filters can have low-pass, high-pass, or band-pass frequency characteristics. CIC filters use only addition and subtraction. FIR filters use addition, subtraction, but most FIR filters also require multiplication. CIC filters have a specific frequency roll-off, while low pass FIR filters can have an arbitrarily sharp frequency roll-off.

CIC filters are in general much more economical than general FIR filters, but tradeoffs are involved. In cases where only a small amount of interpolation or decimation are needed, FIR filters generally have the advantage. However, when rates change by a factor of 10 or more, achieving a useful FIR filter anti-aliasing stop band requires exponentially increasing numbers of FIR taps.

For large rate changes, a CIC has a significant advantage over a FIR filter with respect to architectural and computational efficiency computational efficiency. Additionally, CIC filters can typically be reconfigured for different rates by changing nothing more than the decimation/interpolation section assuming the bit width of the integrators and comb sections meets certain mathematical criteria based on the maximum possible rate change.

Whereas a FIR filter can use fixed or floating point math, a CIC filter uses only fixed point math. This is necessary so that the integrator and comb sections perform complementary discrete mathematical operations. While the reasons are less than intuitive, an inherent characteristic of the CIC architecture is that if fixed bit length overflows occur in the integrators, they are corrected in the comb sections.

The range of filter shapes and responses available from a CIC filter is somewhat limited. Larger amounts of stop band rejection can be achieved by increasing the number of poles. However, doing so requires an increase in bit width in the integrator and comb sections which increases filter complexity. The shape of the filter response provides even fewer degrees of design freedom. For this reason, many real-world filtering requirements cannot be met by a CIC filter alone. However, a CIC filter followed by a short to moderate length FIR or IIR proves highly applicable. Additionally, the FIR filter shape is normalized relative to the CIC's sampling rate at the FIR/CIC interface so one set of FIR coefficients can be used over a range of CIC interpolation and decimation rates.

CIC Filter Applications

CIC filters are well suited for anti aliasing filtering prior to decimation (sample rate reduction), as shown in Figure. This application is associated with very high data rate filtering, such as hardware quadrature modulation and demodulation in modern wireless systems and delta sigma A/D and D/Aconverters.

OVERVIEW OF SDR AND FPGA

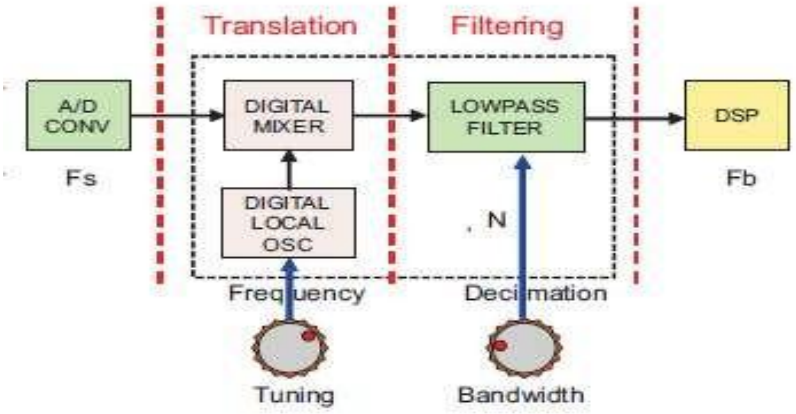


Figure3.1. shows the two-step processing performed by the digital down converter.

Frequency translation from IF down to base band is performed by the oscillator and mixer.
The'' tuning'' knob represents the programmability of the local oscillator frequency to select the desired signal for down conversion to base band.
The base band signal bandwidth is set by setting decimation factor N and low pass FIR filter:
*Base band sample frequency fb=fs/N
*Base band bandwidth=0.8 x fb
The Base band bandwidth equation reflects a typical 80% pass band characteristics, and complex (I+Q) samples.
The"bandwith" knob represents the programmability of the decimation factor to select the desired baseband signalbandwidth.3.1

FPGAs forSDR

Like ASICs, all the logic elements in FPGAs can execute in parallel. This includes the hardware multipliers, and you can now get over 1000 of them on a single FPGA.
This is in sharp contrast to programmable DSPs, which normally have just a handful of multipliers that must be operated sequentially.
FPGA memory can now be configured with the design tool to implement just the right structure for tasks that include dual port RAM, FIFOs, shift registers and other popular memory types.
These memories can be distributed along the signal path or interspersed with the multipliers and math blocks, so that the whole signal processing task operates in parallel in a systolic pipelined fashion.
Again, this is dramatically different from sequential execution and data fetches from external memory as in a programmable DSP.

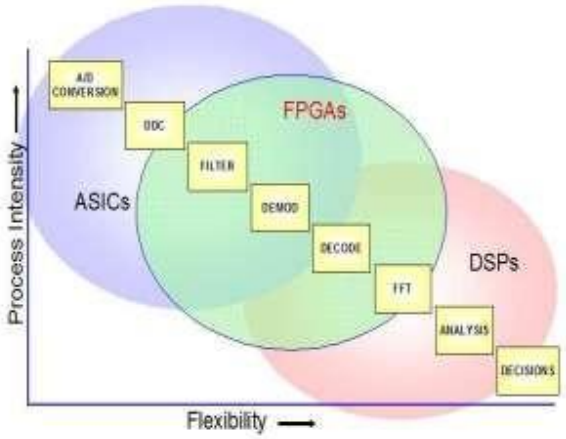


Figure3.2 FPGAs have significantly invaded the Application task space as shown by the center bubble in the task diagram

FPGAs Bridge the SDR Application Space

As a result, FPGAs have significantly invaded the Application task space as shown by the center bubble in the task diagram above. They offer the advantages of parallel hardware tohandle some of the high process-intensity functions like DDCs and the benefit of programmability to accommodate some of the decoding and analysis functions of DSPs.These advantages may come at the expense of increased power dissipation and increased product costs. However, these considerations are often secondary to the Performance and capabilities of these remarkable devices.

Spartan-3E FPGA Family

The Spartan™-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates.

These Spartan-3E enhancements, combined with advanced 90 nm process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry. Because of their exceptionally low cost, Spartan-3E FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment.

The Spartan-3E family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

Applications of FPGAs

FPGAs have gained rapid acceptance and growth over the past decade because they can be applied to a very wide range of applications. A list of typical applications includes: random logic, integrating multiple SPLDs, device controllers, communication encoding and filtering, small to medium sized systems with SRAM blocks, and many more.

Other interesting applications of FPGAs are prototyping of designs later to be implemented in gate arrays, and also emulation of entire large hardware systems. The former of these applications might be possible using only a single large FPGA (which corresponds to a small Gate Array in terms of capacity), and the latter would entail many FPGAs connected by some sort of interconnect; for emulation of hardware. Another promising area for FPGA application is the usage of FPGAs as custom computing machines. This involves using the programmable parts to “execute” software, rather than compiling the software for execution on a regular CPU.

SIMULATION, CHIP SCOPE AND SYNTHESIS RESULTS

CIC based DDC-Simulation results

The CIC filter consists of integrator which implements the accumulator equation as given below.

$$y[n] = y[n-1] + x[n] \quad (5)$$

There is a practial problem in implementing it. If the input signal has any small DC value then it simply accumulates over time and goes to either maximum or minimum value of the 2s complement number. This DC value builds up at the output of integrator, can be seen from the below figure4.1.

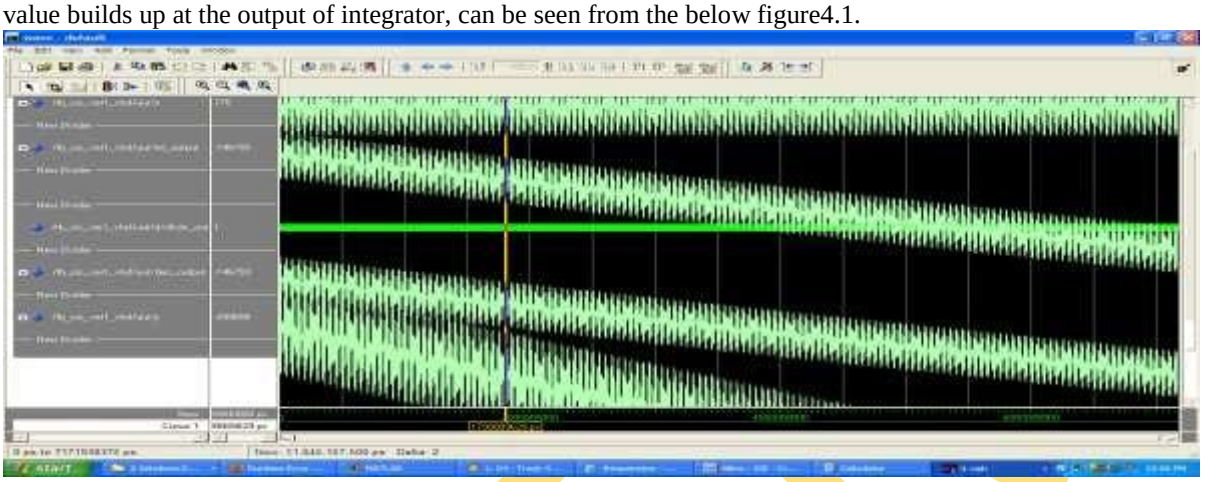


Figure4.1.The DC value builds up at the output of integrator

Hence the gain of feedback term is reduced in the integrator equation to realize a stable filter.
The equation y[n] = 0.5y [n-1] + x[n] is implemented. In this case the output will be stable as shown in below figure.4.2

Final results output

The following two figures show the simulation results obtained for CIC based DDC. Detailed labels are written above each waveform

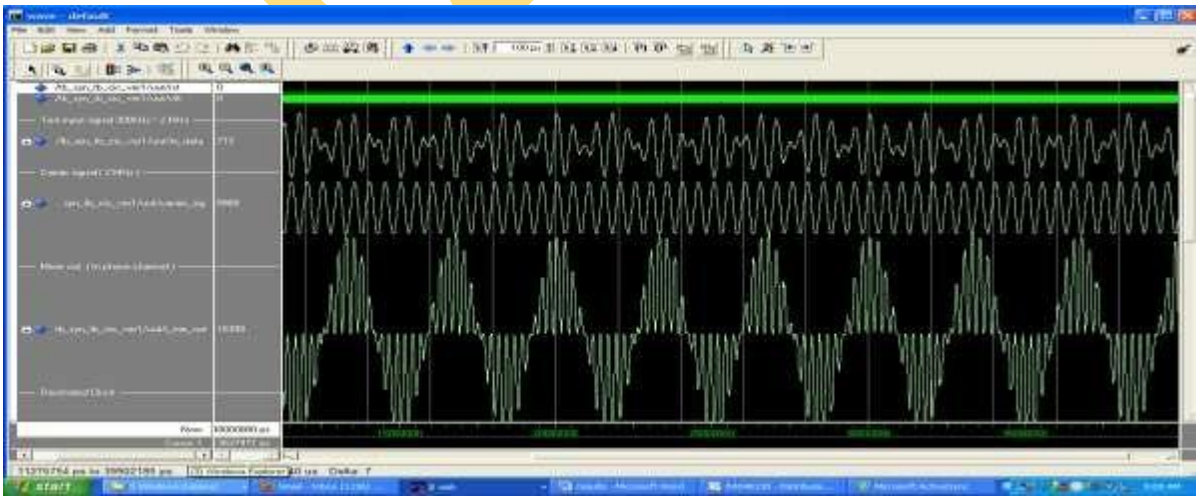


Figure.4.2 the output will be stable as shown

The test input signal is a mixed signal with 300KHz and 2 MHz. This signal is obtained by multiplying two DDS's outputs. This is the first waveform (after rst and clk signals) in the above figure. The second waveform is 2 MHz carrier which is generated with another DDS.

Mixer output for in phase (I) channel

Next waveform is mixer output for in phase (I) channel as shown figure4.3

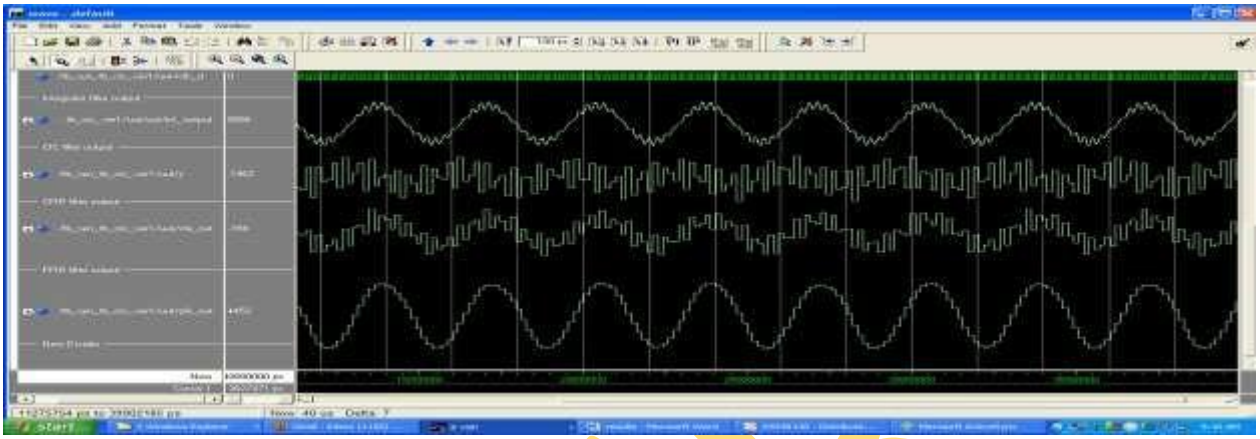


Figure4.3.waveform is mixer output for in phase (I) channel

In the above figure first the decimated clock is shown. This is decimated with a factor of 8. The second figure in above figure is the integrator stage output of CIC architecture. The next waveform is the complete CIC output. We can notice the CIC output is coming with decimated clock.
Next in the figure compensating FIR filter (CFIR) output is shown. This becomes input to programmable FIR (PFIR) filter. The last waveform shows the output of PFIR filter. As expected the 300 KHz base band signal with decimated clock isrecovered.

CIC Based DDC-Chip Scope results

The CIC after porting on FPGA is tested with chip scope. Because of memory limitations on FPGA each stage output is not capture on chip scope. Only the input and output are connected to chip scope data port. The below figure shows the test input signal for DDC which is 300 KHz mixed with 2 MHz carrier. We can notice that the in_data check box is selected in the bus plot.

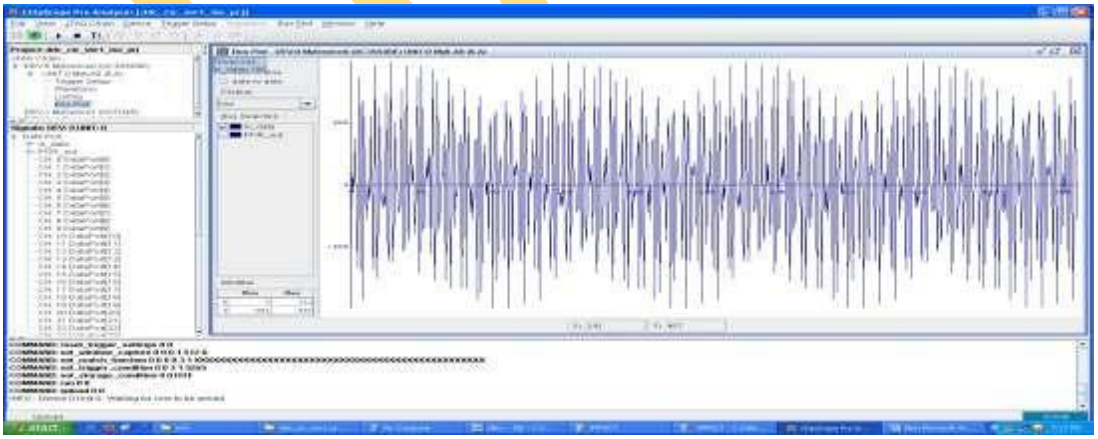


Figure4.4. Shows the test input signal for DDC which is 300 KHz mixed with 2 MHz carrier.

The below figure shows the output of the DDC. Note that the PFIR_out check box is selected in the bus plot. It can be see that the output is 300 KHz sinwave.

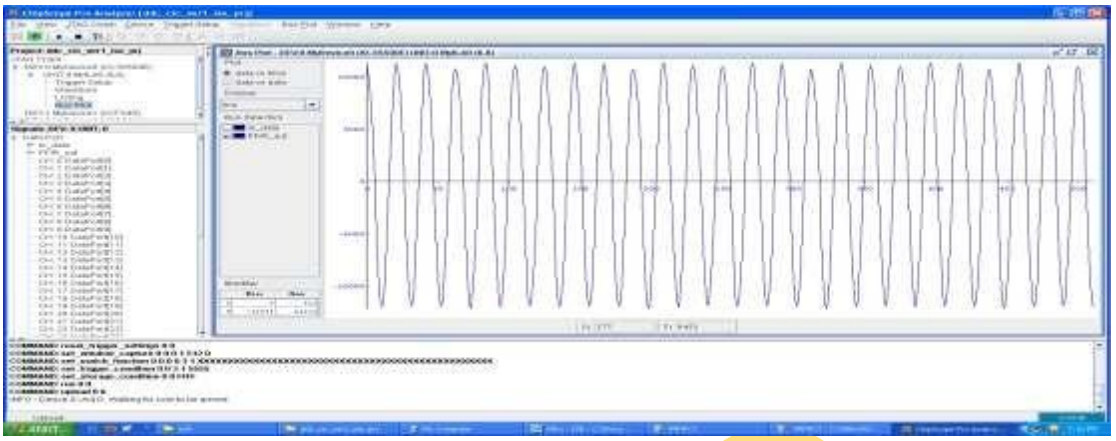


Figure4.5 shows the output of the DDC. The output is 300 KHz sin wave

CIC Based DDC–*Synthesisresults*

Device utilizationsummary:

Selected Device: 3s500efg320-4
Number of Slices: 3320 out of 4656 71%
Number of Slice Flip Flops: 2635out of9312 28%
Number of 4 input LUTs: 5322 out of 9312 57%
Number ofIOs: 50
Number ofbondedIOBs: 26 out of 232 11%
Number of MULT18X18SIOs: 9out of 20 45%
NumberofGCLKs: 3 outof 2412%
NumberofDCMs: 1 outof 425%

Timing Summary:

Speed Grade: -4
Minimum period: 16.196ns
(Maximum Frequency: 61.744MHz)
Minimum input arrival time before clock: No path found
Maximum output required time after clock: 7.245ns
Maximum combinational path delay: 4.733ns

Performance and area comparison of CIC and polyphase structures

Area Comparison as shown in Table1:

Table1.Area Comparison

	CIC Filter	Polyphase Filter
Number of Slices	3320	3966
Number of Slice Flip Flops	2635	2393

Speed Comparison as shown in Table2:

Table2.Speed Comparison

	CIC Filter	Polyphase Filter
Minimum period	16.196ns	11.333ns

Applications

- Front end section of all digital software definedradios
- FPGA based multi rate signal processingsystems.
- Communication systems where the demodulation can be achieved through the mixer actionetc.

Advantages

- Better integration possible by accommodating additional logic on sameFPGA.
- Customization is possible to very highdegree
- FPGA is more suitable for implementing CIC filters etc (with rich set of registers inthem)

VHDL IP can be used for ASIC manufacturingalso

CONCLUSIONS

The issues in designing digital down converter are studied. The main applications where DDC becomes thefront end of software defined radio are understood. Two architectures; CIC based and polyphase based are analyzed and implemented forFPGAs.
VHDL generic coding style is followed to make the blocks highly configurable so that the same design with generic map can be configured for different decimation rates. Stability issues in realizing CIC filters are studied. CIC filter followed by compensating FIR filter are realized to achieve flat magnitude response over pass band. The programmable filter after CFIR is realized to further rejected aliased band due to decimation.
FDA tool is used for generating the filter coefficients for various filters. The inverse SINC function is taken for realizing CFIR filter. Filter coefficients are converted to fixed point and used in VHDL coding.
Polyphase based DDC is also realized with generic coding style. Decimation is achieved with Xilinx digital clock manager (DCM) component.
Simulation and chip scope results are verified for both architectures. The chip scope results are captured at 50 MHz clock speed on Spartan 3E FPGA. The comparison shows polyphase takes more area in comparison with CIC based filter. Timing results show that both work at high frequency. Hence the results are taken with 50 MHz clock onFPGA.
The CIC architecture is suitable when input is coming at very high and required decimation factor is also low. That is for 2 , 4 etc. In this case polyphase architecture becomes difficult. As the filter structures need to run at high frequency.

REFERENCES

[1] A down sample designs under special condition in high speed all digitalsystem.
SUN Hongwei, CHEN Jinshu Dept of Electronic engineering. Tsinghua univ Beijing china
2nd International symposium on IITA -2008 IEEE Computer society, pp 269-273

[2] Design of programmable digital down converter forWiMAX
Charanjit Singh1, Dr. Manjeet Singh Patterh1 ,University College of Engg., Punjabi University; Punjab, India
Indian Journal of Science and Technology Vol.2 No 3 (Mar. 2009) ISSN: 0974- 6846, pp 20-21

[3] CIC filter introduction, *Matthew P.Donadio*

[4] DDC filter Xilinx and Altera application notes

[5] Xilinx FPGA Data sheet for Spartan 3EFPGA.

[6] User guide for Spartan 3E FPGA starterkit.